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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,469	11/08/2001	Sharmin Sadoughi	10200/103	1036

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,469	SADOUGHI ET AL.	
	Examiner	Art Unit	
	Thao P Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-15 and 24-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10,13-15,24,25 and 29-32* is/are rejected.

7)☒ Claim(s) *5-8,11-12,26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Examiner took notice of amendments and remarks received on 1/16/04. The amendments are being considered.

Claim 1 was amended.

Claims 9 and 16-23 were canceled.

Claims 24-32 were newly added.

2. Claims 1-8, 10-15, and 24-32 are pending in this application.

Claim Rejections

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 10,13-15, 24-25, 29-32 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Iyer et al., U.S. Patent No. 6,423,631, and in view of Chang et al., U.S. Patent No. 6,130,146.

Regarding to claim 1, Iyer et al. discloses a process for fabricating a semiconductor structure **(See Figs. 2A-2E and Cols. 1-14)** comprising the steps of:

. depositing a nitride layer **226 (Fig. 2B)** on a semiconductor substrate **200** wherein the nitride layer comprises silicon and nitrogen **(silicon nitride SiN layer 226, Fig. 2B; lines 24-25, Col. 8)**;

. depositing an antireflective layer **206 (Fig. 2C)** on the semiconductor substrate **(lines 39-41, Col. 8);**

wherein the depositing of the antireflective layer **226** comprises reacting SiH_2Cl_2, NH_3, and N_2O (**dichlorosilane** SiH_2Cl_2**, ammonia** NH_3**, and nitrous oxide** N_2O**, lines 44-50, Col. 6).**

However, Iyer et al. fails to disclose the steps of depositing the nitride layer **226** and the antireflective layer **206** using the same tool.

Chang et al. discloses a method of forming nitride layer and antireflective layer using the same tool **(both layers are deposited in the same LPCVD chamber, lines 1-25, Col. 3)**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form both nitride layer and antireflective layer with the same tool

as taught by Chang et al. in the method of Iyer et al. **because** the nitride layer and the antireflective layer are formed using a single reaction tool or the same chamber would reduce the amount of time and number of steps required for forming a semiconductor structure, thus save the process time and cost far less than a two chamber deposition process **(lines 20-25, Col. 2; lines 26-30, Col. 3).**

Regarding to claim 2, Iyer et al. and Chang et al. disclose the claimed limitations as applied for claim 1 above, Iyer et al. further discloses the depositing of the nitride layer occurs before the depositing of the antireflective layer **(Figs. 2B-2C; lines 25-42, Col. 8)**.

Regarding to claim 3, Iyer et al. and Chang et al. disclose the claimed limitations as applied for claim 1 above, Iyer et al. further discloses the depositing of the antireflective layer occurs before the depositing of the nitride layer **210 (Fig. 2D; lines 47-49, Col. 8).**

Regarding to claim 4, Iyer et al. and Chang et al. disclose the claimed limitations as applied for claim 1 above, Chang et al. further discloses wherein the depositing of the nitride layer comprises reacting SiH_2Cl_2, and NH_3 **(lines 5-6, Col. 3)**.

Regarding to claim 10, Iyer et al. and Chang et al. disclose the claimed limitations as applied for claim 1 above, Iyer et al. further discloses wherein the antireflective layer comprises silicon oxynitride **(lines 40-50, Col. 6)**.

Regarding to claim 13, Iyer et al. and Chang et al. disclose the claimed limitations as applied for claim 1 above, Chang et al. further discloses the tool used in claim 1 comprises a low pressure chemical vapor deposition tool (**LPCVD, Abstract, lines 4-20, Col. 3**).

Regarding to claim 14, both Iyer et al. and Chang et al. disclose the process for fabricating a semiconductor device comprising forming a semiconductor structure by the process of claim 1 and forming a semiconductor device from the semiconductor structure (**See Fig. 2F of Iyer et al. and Fig. 2-5 of Chang et al.**).

Regarding to claim 15, both Iyer et al. and Chang et al. disclose the process for making an electronic device comprising forming a semiconductor device by the process of claim 14 and forming the electronic device from the semiconductor device (**See Fig. 2F of Iyer et al. and Fig. 2-5 of Chang et al.**).

Regarding to claim 24, Iyer et al. discloses a process for fabricating a semiconductor structure **(See Figs. 2A-2E and Cols. 1-14)** comprising the steps of:

. depositing a nitride layer **226 (Fig. 2B)** on a semiconductor substrate **200** wherein the nitride layer comprises silicon and nitrogen **(silicon nitride SiN layer 226, Fig. 2B; lines 24-25, Col. 8)**;

. depositing an antireflective layer **206 (Fig. 2C)** on the semiconductor substrate **(lines 39-41, Col. 8);**

wherein the depositing of the antireflective layer **226** comprises silicon-rich nitride (**lines 50-53, Col. 5 and line 31, Col. 6**).

However, Iyer et al. fails to disclose the steps of depositing the nitride layer **226** and the antireflective layer **206** using the same tool.

Chang et al. discloses a method of forming nitride layer and antireflective layer using the same tool **(both layers are deposited in the same LPCVD chamber, lines 1-25, Col. 3)**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form both nitride layer and antireflective layer with the same tool as taught by Chang et al. in the method of Iyer et al. **because** the nitride layer and the antireflective layer are formed using a single reaction tool or the same chamber would reduce the amount of time and number of steps required for forming a semiconductor structure, thus save the process time and cost far less than a two chamber deposition process **(lines 20-25, Col. 2; lines 26-30, Col. 3).**

Regarding to claim 25, Iyer et al. and Chang et al. disclose the claimed limitations as applied for claim 24 above, Chang et al. further discloses wherein the depositing of the nitride layer comprises reacting SiH_2Cl_2, and NH_3 (**lines 5-6, Col. 3**).

Regarding to claim 29, both Iyer et al. and Chang et al. disclose the process for fabricating a semiconductor device comprising forming a semiconductor structure by the process of claim 24 and forming a semiconductor device from the semiconductor structure (**See Fig. 2F of Iyer et al. and Figs. 2-5 of Chang et al.**).

Regarding to claim 30, both Iyer et al. and Chang et al. disclose the process for making an electronic device comprising forming a semiconductor device by the process of claim 29 and forming the electronic device from the semiconductor device (**See Fig. 2F of Iyer et al. and Figs. 2-5 of Chang et al.**).

Regarding to claim 31, Iyer et al. discloses a process for fabricating a semiconductor structure **(See Figs. 2A-2E and Cols. 1-14)** comprising the steps of:

. depositing a nitride layer **226 (Fig. 2B)** on a semiconductor substrate **200** wherein the nitride layer comprises silicon and nitrogen **(silicon nitride SiN layer 226, Fig. 2B; lines 24-25, Col. 8)**;

. depositing a SiO_2 layer on the semiconductor substrate (**silicon-rich oxide, lines 51-53, Col. 5; lines 21-30, Col. 6**).

However, Iyer et al. fails to disclose the steps of depositing the nitride layer **226** and the antireflective SiO_2 layer **206** using the same tool.

Chang et al. discloses a method of forming nitride layer and antireflective layer layer using the same tool **(both layers are deposited in the same LPCVD chamber, lines 1-25, Col. 3)**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form both nitride layer and SiO_2 layer with the same tool as taught by Chang et al. in the method of Iyer et al. **because** the nitride layer and the antireflective SiO_2 layer are formed using a single reaction tool or the same chamber would reduce the amount of time and number of steps required for forming a semiconductor structure, thus save the process time and cost far less than a two chamber deposition process **(lines 20-25, Col. 2; lines 26-30, Col. 3).**

Regarding to claim 32, Iyer et al. and Chang et al. disclose the claimed limitations as applied for claim 31 above, Iyer et al. further discloses wherein the depositing of the oxide layer comprises reacting SiH_2Cl_2, and N_2O **(dichlorosilane SiH_2Cl_2, and nitrous oxide N_2O, lines 25-30, Col. 6).**

Reasons for Indication of Allowable Subject Matter

5. Claims 5-8, 11-12, 26-28 are **objected** to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the

claimed limitations. Iyer et al. (U.S. Patent No6423631) and Chang et al. (U.S. Patent No. 6130146), taken individually or in combination, do not teach the claimed invention including: the volumetric flow rate ratio for dichlorosilane and ammonia is from 0.3 : 1 to 5:1 (claims 5, 26), wherein the nitride layer comprises silicon deficient nitride (claims 6, 27), or silicon rich nitride (claim 7), or a graded silicon nitride layer (claim 8), the process of claims 1 (and claim 24) further comprising depositing an oxide layer on the semiconductor substrate with the same tool that used in claim 1 (and claim 24) (claims 11-12, and 28)

6. When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le